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A General-Purpose Program for Nonlinear Microwave Circuit Design

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Abstract—**The paper describes the basic philosophy and the general structure of a user-oriented program package capable of designing broad classes of nonlinear microwave subsystems. Some of the peculiar aspects of the nonlinear design problem and the computer solutions adopted are discussed in detail. The application to a practical medium-power oscillator shows that the program is numerically efficient and yields well-defined and accurate results. Furthermore it provides full coverage of several aspects of circuit performance that were previously treated by empirical approaches, such as detailed effects of higher harmonics, active device operating temperatures, and circuit regulations.**

I. INTRODUCTION

THE COMPUTER-AIDED design (CAD) of linear microwave circuits can be considered a well-settled matter, as is shown by the extensive technical literature on this subject, and by the commercial availability of powerful general-purpose CAD programs [1]. On the other hand, the general problem of nonlinear circuit design still represents a challenge for the microwave engineer, owing to its much higher difficulty: in fact, in this case, carrying out a design means finding a network and a nonsinusoidal electrical regime which satisfies the design specifications, that this network must be able to support.

The primary purpose of this paper is to describe the structure and basic philosophy, and to illustrate an example of the practical application of a program package allowing straightforward MIC designs to be carried out within a class of active nonlinear subsystems having the general topology shown in Fig. 1. In the current version of this program the nonlinearity is confined to the presence of a user-defined nonlinear "component" having a maximum of 3 ports and usually consisting of a set of semiconductor chips: possible combinations are, for example, one transistor (either bipolar or FET), one or two diodes, or one transistor and one diode. The remaining blocks are representative of linear subnetworks and are labeled according to their physical meaning:

- *L* linear elements (if any) of chip equivalent circuits;
- *S* set of movable short-circuit connections allowing any chip mount configuration to be selected (e.g., common source or gate for an FET chip);
- *P* package or mounting parasitics;
- *M* MIC (usually microstrip) network including load, dc bias, and possibly a number of independent sinusoidal sources harmonically related to the fundamental frequency of operation (e.g., the pump in a frequency divider).

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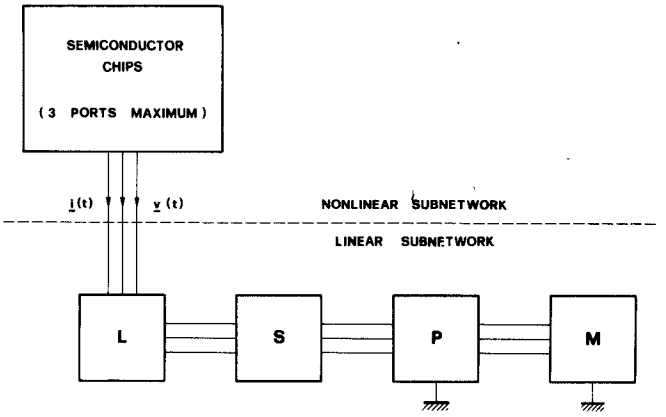

Fig. 1. Schematic topology of microwave nonlinear network.

The topology of the linear subnetwork is completely arbitrary and can be specified by the user in the input data file; in the same way, one can also select a number of physical or electrical parameters of the microstrip network to be used as design variables. Thus despite the limitations on the nonlinear subnetwork, the program is general enough to cover a number of applications of practical interest, including frequency dividers, microwave oscillators both free-running and voltage-controlled, active multipliers, and so on. Furthermore, the basic discussion is equally valid for any number of ports of the nonlinear subnetwork.

The design method is based on the assumption that the semiconductor devices can be described by a reliable nonlinear circuit model, the availability of such models at present being well established as a result of the work of several research teams throughout the world [2]–[5]. Otherwise the formulation is rigorous, at least in principle, and is probably more advanced than many previous approaches to the same problem under several respects. As a first point, all relevant harmonics of the fundamental frequency of operation are exactly accounted for, so that the intrinsic limitations of most available design techniques (e.g., those based on large-signal S-parameters [6], [7]) are overcome. This may be of special importance in the case of power devices acting in a frequency-selective environment such as microstrip circuitry. Furthermore, a straightforward computer solution of the basic problem—designing the nonlinear network for a given set of electrical specifications —becomes feasible and cost-effective thanks to a special optimization strategy [8]. The unknown circuit parameters and the signal waveforms are simultaneously determined by minimizing a unique objective function, thus avoiding the nesting of nonlinear analysis and network optimization loops. The application example presented—concerning the design of a medium-power microstrip oscillator—clearly shows how deep an insight into circuit performance can be obtained by the present approach. The available information includes voltage and current waveforms, junction temperatures, effects of harmonic components, and compensation of the spread of active device parameters by circuit trimming.

II. Design Philosophy

As in any circuit design problem, the starting information is represented by a set of electrical specifications which define the desired network performance. In order to meet the design objectives, a first obvious requirement is that a suitable number of degrees of freedom be available in the linear subnetwork. This is accomplished in the usual way, by selecting a topology of the microstrip network and by choosing some of its electrical or physical parameters as a first set of problem unknowns, namely $\boldsymbol{P}$. Since the network is nonlinear, however, its performance is not only determined by physical configuration, but also depends on the electrical regime that takes place in the circuit. Thus to obtain a complete description we must introduce a further set of unknowns, which generally speaking consist of the voltage and current waveforms. In practical cases one is mostly concerned with the steady-state behavior, so that we may restrict our search to those electrical regimes that the network can support which are periodic in time. The unknowns describing the electrical regime may then be reduced to the vector of (complex) voltage harmonics at the ports of the nonlinear subnetwork, namely $\boldsymbol{V}$. On the other hand, semiconductor devices are usually best simulated in terms of time-domain voltage and current vectors $\boldsymbol{v}(t), \boldsymbol{i}(t)$. A general time-domain representation of the nonlinear subnetwork could be of the form

$$\boldsymbol{i}(t) = \boldsymbol{f}\left\{\boldsymbol{i}(t), \frac{d\boldsymbol{i}}{dt}, \boldsymbol{v}(t), \frac{d\boldsymbol{v}}{dt}\right\} \tag{1}$$

where $\boldsymbol{f}$ is nonlinear and analytically known. Equation (1) is most common, but higher order derivatives could appear as well without affecting the validity of the following discussion. Fig. 2 shows an example drawn from the literature [3] of a nonlinear circuit model for an active device (MSC-3000 chip), leading by inspection to a set of time-domain equations of the form (1).

For any given vector $\boldsymbol{P}$ the frequency-domain equations of the linear subnetwork can be written down as

$$\boldsymbol{I}(\omega) = \boldsymbol{Y}(\omega, \boldsymbol{P})\boldsymbol{V}(\omega) + \boldsymbol{J}(\omega, \boldsymbol{P}) \tag{2}$$

where $\boldsymbol{V}, \boldsymbol{I}$ are vectors of voltage and current phasors at the subnetwork ports, $\boldsymbol{Y}$ represents its admittance matrix, and $\boldsymbol{J}$ is a vector of Norton's equivalent current sources. Assuming a periodic regime with fundamental angular frequency ω_0 we also have

$$\boldsymbol{i}(t) = \mathrm{Re}\left\{\sum_{k=0}^{N} \boldsymbol{I}_k \exp(jk\omega_0 t)\right\}$$

$$\boldsymbol{v}(t) = \mathrm{Re}\left\{\sum_{k=0}^{N} \boldsymbol{V}_k \exp(jk\omega_0 t)\right\} \tag{3}$$

N being the number of significant harmonics. At $\omega = k\omega_0$, (2) is rewritten as

$$\boldsymbol{I}_k = \boldsymbol{Y}(k\omega_0, \boldsymbol{P})\boldsymbol{V}_k + \boldsymbol{J}_k(\boldsymbol{P}). \tag{4}$$

Now we replace (4) into (3) and (3) into (1), and take the

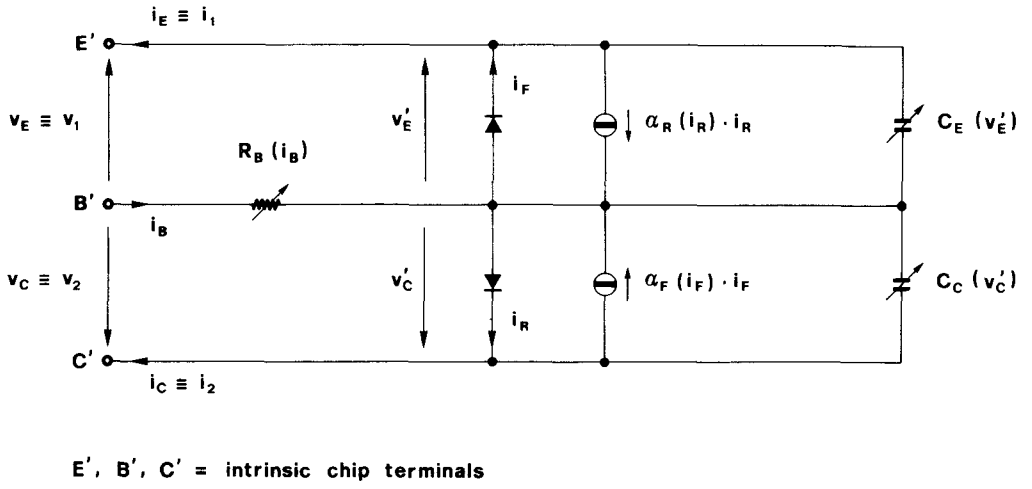

Fig. 2. Nonlinear equivalent circuit of microwave transistor chip (after [3]).

Fourier expansion of the currents to obtain

$$i(t) = \mathrm{Re}\left\{ \sum_{k=0}^{N} \boldsymbol{F}_k(\boldsymbol{V}) \exp(jk\omega_0 t) \right\} \tag{5}$$

where $\boldsymbol{F}_k$ may actually be computed by the FFT. A comparison of (5) and (4) leads to the nonlinear solving system

$$\boldsymbol{F}_k(\boldsymbol{V}) - \boldsymbol{Y}(k\omega_0, \boldsymbol{P})\boldsymbol{V}_k - \boldsymbol{J}_k(\boldsymbol{P}) = \boldsymbol{O}, \qquad k = 0,1,\cdots,N. \tag{6}$$

The above approach is a straightforward application of the well-known harmonic-balance technique [9], [10]. Once a solution of (6) has been found, all quantities used to describe circuit performance (network functions) may be determined by conventional linear network analysis, to be carried out, if required, at several harmonic frequencies.

In summary, the problem to be solved consists of finding the unknowns $\boldsymbol{P}, \boldsymbol{V}$ in such a way that both (6) and the design specifications be satisfied.

It should be noted that the above considerations implicitly assume an order of priority between the two sets of unknowns, in that physically significant network functions and thus an objective function for optimization can only be found after solving the nonlinear system (6). This leads to a solution scheme consisting of two nested iteration loops, the inner one providing the objective function for the outer.

Now one of the key ideas underlying the present design approach is that this apparent hierarchy of variables can be bypassed. As a first point, we observe that solving the nonlinear system (6) is conceptually equivalent to minimizing the harmonic-balance error

$$e_B(\boldsymbol{P}, \boldsymbol{V}) = \left\{ \sum_{k=0}^{N} |\boldsymbol{F}_k(\boldsymbol{V}) - \boldsymbol{Y}(k\omega_0, \boldsymbol{P})\boldsymbol{V}_k - \boldsymbol{J}_k(\boldsymbol{P})|^2 \right\}^{1/2} \tag{7}$$

with respect to the voltage harmonics (note that from a physical standpoint a solution is only acceptable when the corresponding minimum is zero). On the other hand, the network functions can be computed (in the way described in detail in Section III) starting from *any* given set of design variables $(\boldsymbol{P}, \boldsymbol{V})$ even though not satisfying the network equations (6). In such cases, of course, they are devoid of physical meaning, since the network defined by $\boldsymbol{P}$ cannot support the steady-state regime represented by $\boldsymbol{V}$. They can, nevertheless, be used to define in a purely mathematical sense an objective function encompassing the design specifications. We may thus carry out a simultaneous search for the network parameters and the voltage harmonics by minimizing a suitable combination of such a function and of the harmonic-balance error (7). After a successful optimization the harmonic balance will be restored, and the network functions will get back their original physical meaning, thus providing a significant design with a dramatic saving of computer time.

In fact, there are also very good reasons why the above mentioned hierarchy of variables *should* be bypassed. In several cases of practical interest—usually circuits providing power transfer from one frequency to another such as oscillators or frequency dividers—the solving system (6) turns out to be impossible for a wide variety of linear subnetworks. In such cases a conventional optimization scheme might be severely inefficient or even useless at all unless a starting point close enough to the final solution were available. On the contrary, the present method simply starts with a large harmonic-balance error thus compelling the minimization algorithm to approach network configurations compatible with the desired electrical performance.

III. Formulation of the Objective Function

A considerable effort has been spent in order to make the program as general and flexible as possible, while preserving its user-oriented character. Of course, the standard definitions of the function to be minimized, which are used in conventional linear CAD programs, are not applicable, due to the peculiar aspects of the nonlinear design problem. In this section, we illustrate the solutions that were adopted to cope with such peculiar requirements. The topics to be covered include the computation of network

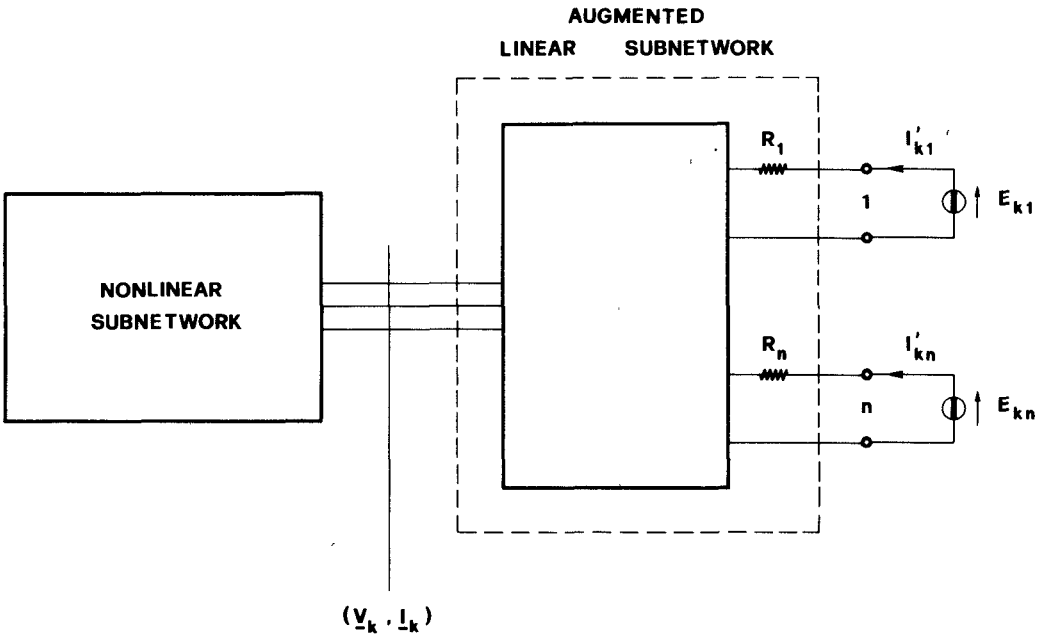

Fig. 3. Modified network topology for computation of network functions.

functions, the formulation of the objective, and the search for operating temperatures of the semiconductor devices. In any case, the starting point will be represented by a set of problem unknowns $(\boldsymbol{P}, \boldsymbol{V})$ provided by the minimization algorithm at any iteration of the search loop.

A. Network Functions

The calculation of network functions usually requires a knowledge of the current harmonics in a number of branches of the linear subnetwork which may, or may not, contain a sinusoidal source (including dc bias for $\omega = 0$). To obtain this, we first modify the topology of the linear subnetwork in such a way that all branches containing free generators and all branches used to compute the network functions are explicitly put into evidence, as shown in Fig. 3. The number of these branches (which will be named "external" branches) is denoted by n, and the number of ports of the nonlinear subnetwork (device ports) by n_D. In this way, we generate an $(n_D + n)$-port circuit which will be referred to as the "augmented" linear subnetwork. To define circuit topology at the data-entry level, we separately input a description of the augmented linear subnetwork to be handled by a general-purpose linear multiport analysis routine, and a set of vectors $\boldsymbol{E}_k$ $(k = 0,1,\cdots,N)$, each containing the free generator voltages at $\omega = k\omega_0$ ($\boldsymbol{E}_k$ is an n-element vector). It is essential that the linear-analysis subprograms allow the circuit to be described on a node basis, since some of the device ports may be floating (e.g., Fig. 4).

In order to carry out one function evaluation, the augmented linear subnetwork is first analyzed at all harmonics of interest, that is, for $\omega = k\omega_0$ $(k = 0,1,\cdots,N)$ to find its admittance matrix $\boldsymbol{Y}_A(k\omega_0, \boldsymbol{P})$. We may write

$$\boldsymbol{Y}_A(k\omega_0, \boldsymbol{P}) = \left[\begin{array}{c|c} \boldsymbol{Y} & \boldsymbol{Y}_{12} \\ \hline \boldsymbol{Y}_{21} & \boldsymbol{Y}' \end{array}\right](k\omega_0, \boldsymbol{P}) \tag{8}$$

where $\boldsymbol{Y}(k\omega_0, \boldsymbol{P})$ is the same admittance matrix appearing in (4). From the augmented subnetwork equations we further get

$$\begin{aligned} \boldsymbol{J}_k(\boldsymbol{P}) &= \boldsymbol{Y}_{12}(k\omega_0, \boldsymbol{P})\boldsymbol{E}_k \\ \boldsymbol{I}_k'(\boldsymbol{P}, \boldsymbol{V}) &= \boldsymbol{Y}_{21}(k\omega_0, \boldsymbol{P})\boldsymbol{V}_k + \boldsymbol{Y}'(k\omega_0, \boldsymbol{P})\boldsymbol{E}_k \end{aligned} \tag{9}$$

where $\boldsymbol{I}_k'$ is the vector of currents in the external branches at $\omega = k\omega_0$; from $\boldsymbol{I}_k'$ and $\boldsymbol{E}_k$ one can derive all network functions which are usually of interest. Note that (8) and (9) also provide a complete description of the linear subnetwork, thus allowing the harmonic-balance error to be computed in the way shown in the previous section.

As an example, let the nonlinear network be a free-running sinusoidal oscillator, whose performance is described in terms of output power (P_o), dc to RF conversion efficiency (η), and harmonic content of the output waveform. In this case, we take $n = 3$, and let the first of the external branches be the load branch and the remaining ones be bias branches (e.g., Fig. 4). Since no free generators other than dc act in the circuit, we have $\boldsymbol{E}_k = 0$ $(k > 0)$ and

$$\boldsymbol{E}_0 = \begin{bmatrix} 0 \\ E_{02} \\ E_{03} \end{bmatrix}. \tag{10}$$

Thus, the network functions may be computed as

$$\begin{aligned} P_0 &= \frac{1}{2} R_1 |I_{11}'|^2 \\ \eta &= \frac{R_1 |I_{11}'|^2}{2\left(E_{02} I_{02}' + E_{03} I_{03}'\right)} \\ S &= 10 \log_{10} \frac{|I_{11}'|^2}{\sum_{k=2}^{N} |I_{k1}'|^2} \end{aligned} \tag{11}$$

where S is the harmonic output power expressed in decibels below the fundamental.

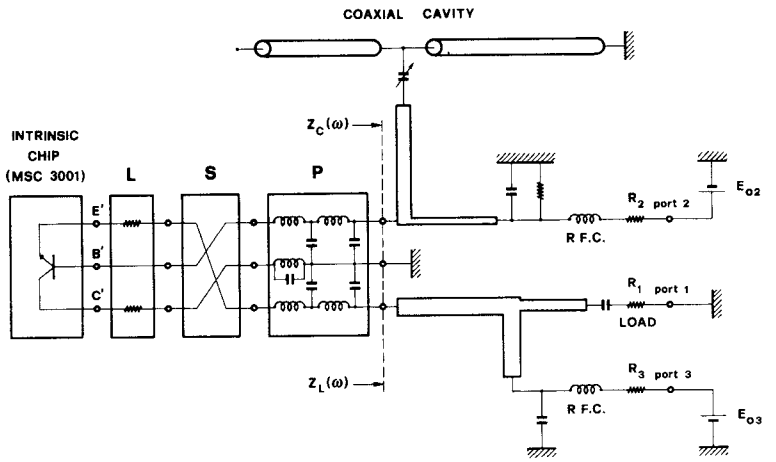

Fig. 4. Circuit diagram of MIC medium-power oscillator.

In conclusion, for any set of design variables $(\boldsymbol{P}, \boldsymbol{V})$ the analysis of the augmented linear subnetwork through (8) and (9) provides all the information required to find the network functions. In practice the program performs this analysis automatically and makes the vectors $\boldsymbol{I}_k'$ available to the user via a COMMON block; the functions are then computed in a user-defined subroutine to ensure maximum flexibility.

B. Objective

For a given set $(\boldsymbol{P}, \boldsymbol{V})$, let $f_i(\boldsymbol{P}, \boldsymbol{V})$ denote any network function used to specify the design goals. The performance specifications will be of the general form

$$f_i(\boldsymbol{P}, \boldsymbol{V}) \geqslant f_{i\min} \qquad i = 1, 2, \cdots, M \tag{12}$$

where $f_{i\min}$ is a suitably selected lower bound. While (12) represents the most commonly encountered case, it is occasionally required that some of the network functions be optimized in a strict sense, i.e., take the maximum possible value in the final circuit, the exact amount being *a priori* unknown. In such cases, we must combine (12) with the further requirements

$$f_i(\boldsymbol{P}, \boldsymbol{V}) \text{ as large as possible}, \qquad i = 1, 2, \cdots, T \quad (T \leqslant M). \tag{13}$$

Besides (12) and (13) the harmonic-balance condition $e_B = 0$ must be imposed. For practical purposes, this is replaced by

$$e_B \leqslant e_{\max} \tag{14}$$

where $e_{\max}$ is a threshold value to be established by experience in relation with the given problem.

In order to define the objective, we first introduce the weighted errors

$$E_0 = W_B(e_B - e_{\max})$$
$$E_i = W_i(f_{i\min} - f_i), \qquad i = 1, 2, \cdots, M \tag{15}$$

(all W's are positive quantities), and let

$$E = \max(E_i), \qquad i = 0, 1, \cdots, M \tag{16}$$

$$\delta_i = \begin{cases} 1, & (E_i > 0) \\ 0, & (E_i \leqslant 0). \end{cases} \tag{17}$$

Now we take as the objective function to be minimized the quantity

$$F_{OB}(\boldsymbol{P}, \boldsymbol{V}) = \begin{cases} \sum_{i=0}^{M} \delta_i E_i^2, & (E > 0) \\ -\sum_{i=1}^{T} E_i^2, & (E \leqslant 0) \end{cases}. \tag{18}$$

When $E \leqslant 0$ the harmonic-balance condition (14) is met, and so are the electrical specifications (12); thus the efforts of the optimization algorithm are entirely devoted to increasing the magnitude of the errors E_i $(i = 1, 2, \cdots, T)$, that is, to making the network functions (13) as large as possible. Note that the introduction of a harmonic-balance threshold $e_{\max} > 0$ is essential whenever design specifications of the kind (13) are to be dealt with. Otherwise one always has $E_0 > 0$, so that any network function exceeding the prescribed lower bound has no further effect on the objective; thus in the long run the program will only try to minimize the harmonic-balance error while keeping all network functions essentially constant at their lower bounds. The above approach has proven effective in optimizing some aspects of circuit performance such as the output power and/or efficiency of an oscillator.

C. Device Temperatures

The temperature of operation usually affects the performance of semiconductor devices in a significant way. This results in temperature-dependent parameters appearing in the chip equivalent circuits, such as the voltage–current relationships of the emitter and collector junctions for the bipolar transistor of Fig. 2. Thus especially for CW operation of power devices, the actual device temperature must be evaluated, in order that the final design be practically significant. Of course a possible approximate solution

would be to give rough *a priori* estimates of the device temperatures and use these to model the equivalent circuits throughout the optimization. However, an accurate determination of the actual temperatures is possible within the present framework at virtually no extra cost in terms of CPU time.

Let us consider any one of the semiconductor devices included in the nonlinear subnetwork, and let $\boldsymbol{V}_{Dk}, \boldsymbol{I}_{Dk}$ be the vectors of voltage and current harmonics at the device ports for $\omega = k\omega_0$ $(k = 0,1,\cdots,N)$, the positive directions for currents being specified in Fig. 1. $\boldsymbol{V}_{Dk}, \boldsymbol{I}_{Dk}$ are obviously subsets of $\boldsymbol{V}_k, \boldsymbol{I}_k$ as defined by (3). Prior to each evaluation of the objective, starting from the given set of design variables $(\boldsymbol{P}, \boldsymbol{V})$ we compute the quantity

$$P_{DJ} = -\boldsymbol{V}_{D0}^T \boldsymbol{I}_{D0} - \frac{1}{2}\sum_{k=1}^{N} \mathrm{Re}\left\{\boldsymbol{V}_{Dk}^T \boldsymbol{I}_{Dk}^*\right\} \tag{19}$$

(we denote by ^{T} a transposed matrix and by * the complex conjugate). If $(\boldsymbol{P}, \boldsymbol{V})$ were a solution of (4) and (6), P_{DJ} would obviously represent the power dissipated inside the device being considered. In general, this will not be the case during the search, but will become true after a successful optimization. Based on (19) we may now introduce the quantity

$$T_D = \begin{cases} T_A, & P_{DJ} \leqslant 0 \\ T_A + R_D \cdot P_{DJ}, & P_{DJ} > 0 \end{cases} \tag{20}$$

where T_A is room temperature and R_D the known thermal resistance of the device being considered. T_D is conventionally used as the current device temperature to compute the temperature-dependent features of the equivalent circuit. Once again, after a successful optimization T_D will represent the actual steady-state temperature of the chip, so that the nonlinear constraints imposed by the device will be exactly formulated in the final description of the circuit.

IV. A Design Example

In this section we report a few numerical and experimental results concerning a medium-power low-noise microstrip oscillator that was designed by means of the computer program described above. This oscillator had to be mechanically tunable over the 2.25 to 2.50-GHz band with a minimum output power of 0.5 W and harmonics lower than −25 dBc. In order to meet the tuning requirements and the very stringent specifications on noise, a tunable coaxial cavity was used and was connected to the transistor base via a capacitive coupling and a microstrip transformer. The selected transistor was an MSC 3001 chip (consisting of two MSC 3000's connected in parallel) in a grounded-bar package for which an accurate circuit model was available. Mainly for the sake of thermal dissipation, a common-collector configuration was adopted; on the emitter side the transistor was matched to the load by a simple microstrip stub network. A complete circuit diagram is shown in Fig. 4, where the main building blocks are labeled according to Fig. 1 and the network topology is arranged according to Fig. 3. A unique bias voltage $E_{02} = E_{03} = -16$ V was used due to system requirements.

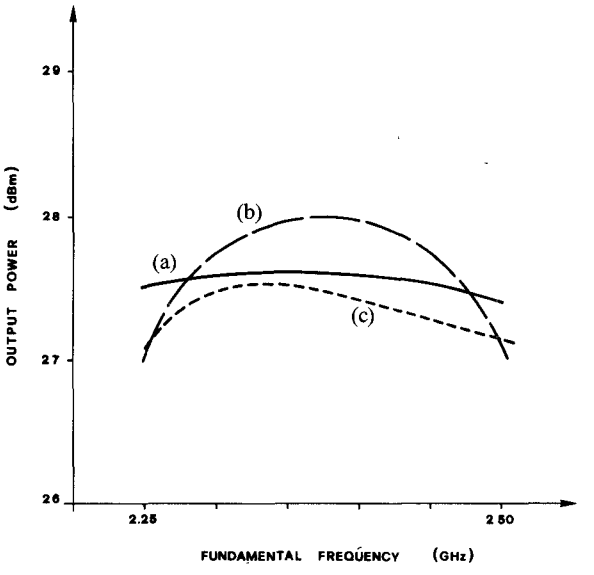

Fig. 5. Oscillator output power versus frequency. (a) Nominal design. (b) Same with a different chip. (c) Measured on prototype.

The design was carried out by optimizing all significant parameters of the passive network (including the bias circuit) as well as three voltage harmonics besides the fundamental and dc components. A circuit model of the chip was obtained by connecting in parallel two identical networks, each having the topology given in Fig. 2. The oscillator performance in terms of output power versus frequency (the latter being determined by mechanical tuning) is shown in Fig. 5. Curve (a) in this figure represents the nominal design, while curve (b) was obtained by dropping the nonlinear model of a different chip [3] into the same linear network. Finally curve (c) is experimental, and was measured on a prototype oscillator built on the basis of the theoretical design. The agreement among these curves gives a clear check of the reliability of our design approach. Other features of the oscillator were a minimum efficiency of 25 percent and a harmonic output power of less than −26.5 dBc across the tuning band, closely corresponding to the predicted values.

The power output capabilities of this circuit were investigated in some detail both numerically and experimentally. Some results concerning the center-band frequency are reported below. In Fig. 6 we plot the load impedance at the fundamental $Z_L(\omega_0)$ (see Fig. 4), which is required to produce a prescribed output power (thick solid curves). This impedance is taken as representative of the microstrip network topology. The interesting point is that $Z_L(\omega_0)$ is almost power-independent in a broad range of power values, roughly 15–28 dBm, while it changes rapidly outside this range. Fig. 7 shows that the cavity impedance $Z_c(\omega_0)$ (see Fig. 4) is virtually a short circuit irrespective of output power, while the solid line in Fig. 8 gives the computed relationship between the output power and the emitter bias resistance (R_3 in Fig. 4). In Fig. 6 we also report the actual $Z_L(\omega_0)$ measured on the prototype oscillator, which is obviously represented by a couple of horizontal straight lines since it is power independent. This

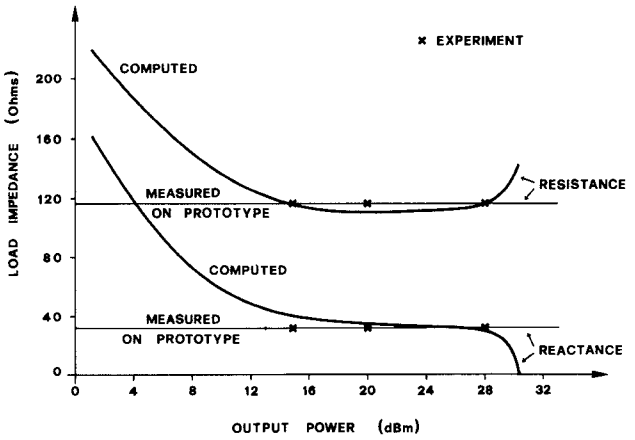

Fig. 6. Load impedance at the fundamental versus output power.

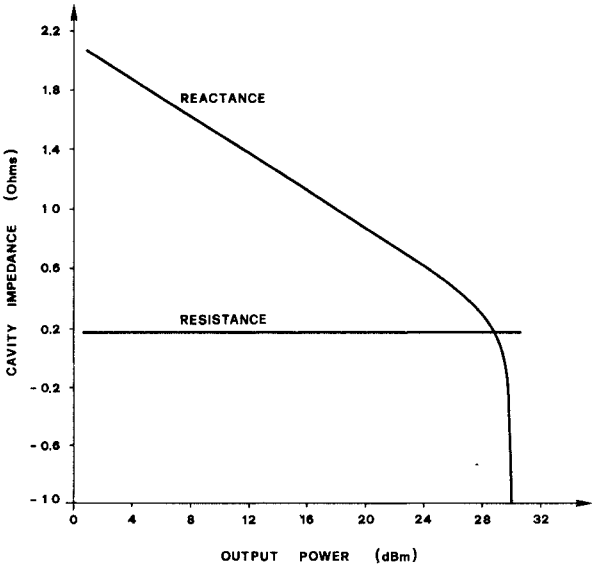

Fig. 7. Cavity impedance at the fundamental versus output power (computed).

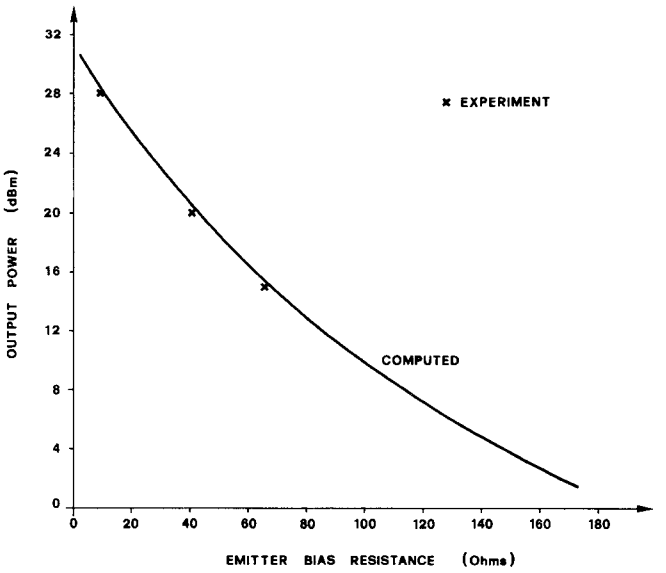

Fig. 8. Dependence of output power on emitter bias resistance.

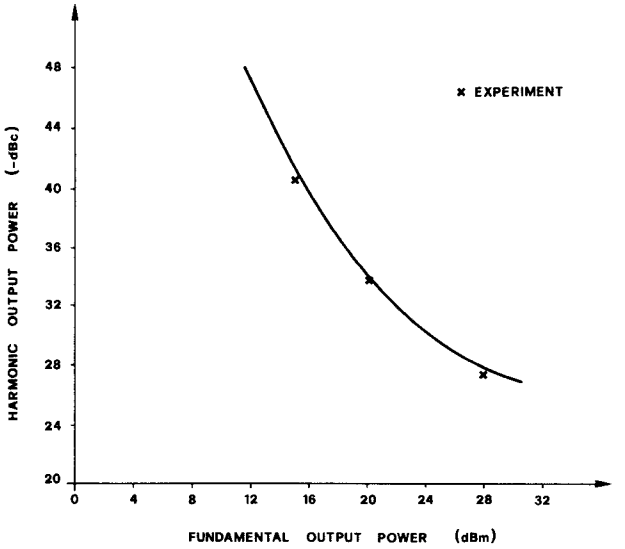

Fig. 9. Spectral purity of output waveform versus power.

impedance is practically the same as the load required for oscillation between 15 and 28 dBm. As a consequence, the oscillator output power could actually be varied throughout the range of constant impedance by simply changing the emitter bias resistance (see the experimental points reported in Figs. 6, 8, and 9): outside the oscillation would cease or else be transferred to spurious frequencies unrelated to ω_o. The above behavior allowed the output power fluctuations due to the spread of the active devices to be compensated by simply trimming the emitter resistor in a production series of about 200 similar oscillators. Finally, Fig. 9 shows the degradation of the spectral purity of the output signal as a function of the fundamental-frequency power output.

The importance of taking into account several harmonics in the design is demonstrated by the data collected in Table I still concerning oscillation and center band. The $N = 4$ column in this table represents the nominal design, which is seen to reproduce very accurately the measured performance, also given in the table. On the other hand,

TABLE I

	Measured	Computed, N = 4	Computed, N = 1
DC to RF conversion efficiency	26%	26.5%	47%
Fundamental power output	27.5 dBm (560 mW)	27.6 dBm (575 mW)	29.4 dBm (870 mW)
Load impedance at ω_o	115 + j 35 Ω	116 + j 33 Ω	95 + j 50 Ω

the $N = 1$ column displays the computed performance when the network is optimized (with the bias circuit kept fixed) while considering only the fundamental and dc components. The results show that the single-frequency design is only moderately misleading concerning the microstrip net-

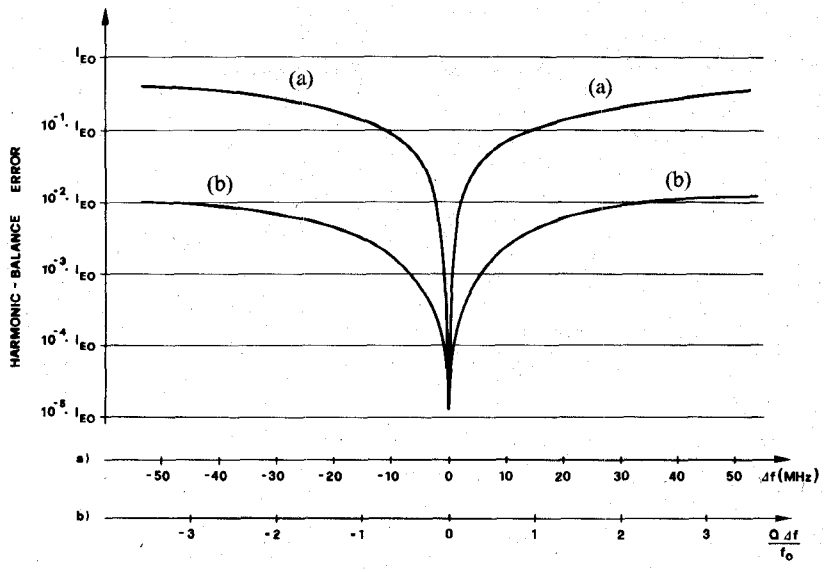

Fig. 10. Minimum harmonic-balance error versus frequency offset. (a) Upper frequency scale. (b) Lower scale.

work, but does not allow the oscillator output power and efficiency to be predicted with practically useful accuracy.

Finally, Fig. 10 shows that the numerical solutions are very well defined with respect to frequency changes. In this figure we plot the minimum harmonic-balance error that the search algorithm can achieve by optimizing the voltage harmonics only with a fixed linear subnetwork (corresponding to the nominal design of the oscillator). Since the error is dimensionally a current, the e_B axis is graduated in terms of fractions of the dc component of the emitter current (I_{E0}) for ease of comparison. Curve (a), corresponding to the upper frequency scale, shows the error as a function of frequency offset from the nominal center-band in megahertz. Curve (b) is the same as (a) but is redrawn with an expanded frequency scale (lower scale) for which one division corresponds to the 3-dB bandwidth of the oscillator cavity. The minimum error (at the nominal frequency of oscillation) is obviously not zero due to numerical roundoff. However, e_B increases by about 2 orders of magnitude in $\pm$ one half of the 3-dB bandwidth and by almost 3 orders of magnitude in ± 2.5 MHz. Thus the design shows no appreciable numerical uncertainty on the actual frequency of oscillation.

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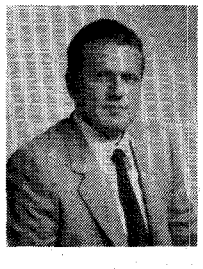

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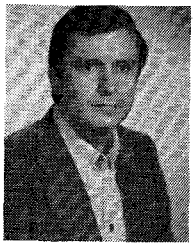

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Short Papers

Higher Order Modes in Square Coaxial Lines

L. GRUNER, MEMBER, IEEE

Abstract—**The cutoff frequencies of higher order modes in square coaxial lines are presented and compared with those of circular coaxial lines having the same mean circumference. It is noted that while the characteristics of the dominant TE_{10} mode and the next TE_{11} mode in the square line differ but little from those of their circular counterparts, the same conclusions do not hold in general for the remainder of the mode spectrum.**

It is well known that a pair of independent waves having a horizontal and a vertical polarization may be supported by waveguides having either a circular or a square cross section. The same conclusion holds for circular coaxial lines as well as square coaxial lines.

While circular coaxial lines have been used extensively in the past, square coaxial lines may be preferable in some applications if a) the presence of flat rather than circular surfaces offers mechanical advantages, and b) it is desired to have an unambiguously defined plane of polarization. Moreover, it may be conjectured that in practice, at least in some instances the cross-polarization ratio, or ability to discriminate against waves having the undesired alternative polarization, may be superior for square lines.

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The higher order mode spectrum of circular coaxial lines is very well known [1]. This may be contrasted with the fact that published information pertaining to square lines is very incomplete and inadequate for most purposes. Thus a method for the determination of the lowest (TE_{10} or TE_{01}) eigenvalues of transmission lines having rectangular inner and outer conductors has been described [2] but no explicit information applicable to square lines is available. The paper by Brackelmann *et al.* [3] deals with rectangular lines comprising inner and outer conductors, the centers of which do not necessarily coincide and which include coaxial lines as a special case; from the curves, a few selected values of the cutoff frequencies of a few modes of square coaxial lines may be deduced. Tourneur [4] arrived at the higher order mode spectrum of a square coaxial line using a finite element method and a variational Rayleigh–Ritz procedure with a polynomial approximation; published information is confined to curves of the cutoff frequencies of the TE_{10}, TE_{11}, TE_{20}, and TM_{11} modes for b/a ratios ranging from 0 to 0.3. Finally, the author has independently described [5]–[7] a technique based on field matching (just as in papers by Bezlyudova and Brackelmann *et al.* [2] and [3], but differing in implementation), applicable to rectangular coaxial lines.

The same computer program which was used to arrive at the higher order mode spectrum of rectangular coaxial lines having arbitrary inner and outer conductor dimensions, has been utilized to deduce the characteristics of square coaxial lines. Calculations were performed for aspect ratios b/a ranging from 0 to 0.95 and the results extrapolated to include $b/a = 1$; it may be noted that

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